ABSTRACT OF THE DISCLOSURE

A part of a scan path lying in the x th stage of a test circuit is formed by successively connecting the FF11x standing at the head of the xth stage to the FF1mx standing at the end of the same in series. The scan path connects the scan input SIN with the input terminal of the FF11n standing at the head of the n th stage, and successively connects the FFs arranged in the second to (n-1) th stages in series, after restarting from the output terminal of the FF1mn standing at the end of the n th stage. The output terminal of the FF1m(n-1) standing at the end of the (n-1) th stage is connected with the input terminal of the FF111 standing at the hed of the first stage, and, finally, the output terminal of the FF1m1 standing at the end of the first stage is connected with the scan output SOT.